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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,023	08/31/2000	Yasuhiro Wakimoto	P108391-00011	4533

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EXAMINER
CHOI, WOO H

ART UNIT	PAPER NUMBER
2186	9

DATE MAILED: 07/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,023	WAKIMOTO, YASUHIRO	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama *et al.* (US Patent Application Publication # US 2001/0003199 A1, hereinafter "Marayuma") and Dye (US Patent # 6,173,381) in view of Lopez-Aguado (US Patent No. 5,586,283).

4. With respect to claims 1, 4, 7, and 12, Maruyama discloses a microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected that comprises:

an address conversion unit (figure 1) which assigns a physical address of a first memory unit (12 and 13) out of the plurality of memory units to a logical address of a load module stored in the first memory unit (figure 3), wherein said load module includes instructions and data (12 stores program which is well known in the art to include instruction and data, 13 stores font which is data); and

a copying unit which copies an instruction code from the load module stored in the first memory unit to a second memory unit of the plurality of memory units (claim 2); and

an address conversion unit which assigns a physical address of the second memory unit (14) to a logical address of the instruction code to the second memory unit (figure 3).

However, Maruyama does not disclose the use of two address conversion units to assign physical addresses of the first and the second memory units to their respective logical addresses. On the other hand, Dye teaches us the use of two address conversion units (Dye, figure 3, 140a and 140b, see also figure 4 and col. 11, lines 43 – 50, where a dual memory control unit generates two sets of physical addresses) to control multiple memory units (col. 10. lines 55 – 59, 140a controls system memory 110 and 140b controls a frame buffer 141, also see figure 4, where multiple banks of memory are controlled by the dual memory controller).

It would have been obvious to one of ordinary skill in the art, having the teachings of Maruyama and Dye before him at the time the invention was made, to include the dual address conversion unit teaching of the memory microprocessor with address conversion units and multiple memory units of Dye in the design of the microprocessor with an address conversion unit and multiple memory units of Maruyama, in order to be able to address a large amount of memory (Dye, col. 11, lines 43-50) that may be required for image processing.

Maruyama and Dye disclose all of the limitations discussed above. However they do not disclose that each of the address conversion units comprises a comparator that compares a

requested logical address with said logical address assigned with said physical address of the respective memory units. On the other hand, Lopez-Aguado discloses an address conversion unit that comprises a comparator that compares a requested logical address with said logical address assigned with said physical address of the respective memory units (col. 5, lines 58 – 66).

It would have been obvious to one of ordinary skill in the art, having the teachings of Maruyama, Dye, and Lopez-Aguado before him at the time the invention was made, to include the address comparator teaching of address conversion units of Lopez-Aguado in the design of address conversion units of Maruyama and Dye, in order to provide for the performance of table walks in a translation lookaside buffer with reduced latency (Lopez-Aguado, col. 2, lines 22 – 24).

5. With respect to claims 2, 5, 8, and 13, the address conversion unit assigns the physical address of the first memory unit to the logical address of the load module and the physical address of the second memory unit to the logical address of the instruction code (Maruyama, figure 3).

6. With respect to claims 3, 6, 9, and 14, the first memory unit includes data for image processing and instruction code for image processing (page 3, paragraph 42, line 9-13)

7. With respect to claims 10, 11, 15, 16, and 17 the speed of the second memory module is faster than the first memory module (page 1, paragraph 9, lines 1-2) and the second memory is constituted of a synchronous DRAM (figure 1).

Response to Amendment

8. Claim 18 has been cancelled. Corresponding rejection is withdrawn.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 4, 7, and 12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

whc
July 12, 2003

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100